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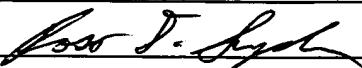
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## PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

1400.4100290

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on 11-22-2006

Signature Typed or printed name Ross D. Snyder, Reg. No.  
37,730Application Number  
09/746,601Filed  
12-21-2000

First Named Inventor

James S. McCormick et al.

Art Unit

2616

Examiner

Scheibel, Robert C.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

 applicant/inventor. assignee of record of the entire interest.  
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96) attorney or agent of record.  
Registration number 37,730 attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 \_\_\_\_\_



Signature

Ross D. Snyder

Typed or printed name

(512) 347-9223

Telephone number

11-22-2006

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.  
Submit multiple forms if more than one signature is required, see below\*.

\*Total of \_\_\_\_\_ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): James S. McCormick, et al.

Title: BUFFERING SYSTEM FOR USE IN A COMMUNICATION SWITCH THAT INCLUDES A MULTIPROCESSOR CONTROL BLOCK AND METHOD THEREFORE

App. No.: 09/746,601 Filed: 12-21-2000

Examiner: Scheibel, Robert C. Group Art Unit: 2616

Atty. Dkt. No. 1400.4100290

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Mail Stop AF  
Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Dear Sir:

Claims 1-23 are pending in the present application. The Examiner has rejected claims 1, 2, 12, 13, 17, and 19-23. The Examiner has objected to claims 3-11, 14-16, and 18. Appellant respectfully requests reconsideration of pending claims 1-23. Appellant files herewith a notice of appeal. Pursuant to the "New Pre-Appeal Brief Conference Pilot Program," 1296 Off. Gaz. Pat. Office 67 (July 12, 2005) and the "Extension of the Pilot Pre-Appeal Brief Conference Program" dated 1/10/2006, Appellant submits a pre-appeal brief request for review. The review is requested for the reasons set forth below:

Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection. Appellant submits the Examiner's "Response to Arguments" provides evidence that the Examiner has failed to consider the pending claims as required by the Manual of Patent Examining Procedure (MPEP) and prevailing case law. MPEP § 2141 sets forth the Graham inquiries for a rejection under 35 U.S.C. § 103. MPEP § 2143 describes basic requirements of a *prima facie* case of obviousness under 35 U.S.C. § 103. As Appellant describes in detail below, Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection.

The Examiner has rejected claims 17, 19, and 21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,253,248 to Dravida et al. in view of Applicant's admitted prior art. Applicant submits that Dravida et al. states, in col. 11, lines 38-43, "The output of congestion monitor 2740 controls nodal processor 2730 such that a primary route to a destination is selected from table 2750 in the absence of congestion and an

alternate route to a destination is selected from table 2760 in the presence of congestion.” However, Applicant submits that Dravida et al. fails to disclose “such that calls are routed away from the congestion.”

Regarding claims 17 and 19, Applicant submits the cited portions of the cited reference fail to render obvious, as one example, “...a plurality of line cards operably couple to the routing control block, wherein each of the line cards includes at least one transmit queue, wherein when congestion is detected on a transmit queue, a congestion indication is provided to the routing control block such that calls are routed away from the congestion.” As another example, Applicant submits the cited portions of the cited reference fail to render obvious “detecting congestion in a transmit queue corresponding to a line card of the communication switch.” The Examiner acknowledges, “Dravida does not expressly disclose the limitation that the input and output buffers are line cards.” The Examiner cites Figure 1 of the present application as indicating “the use of a plurality of line cards in a communications switch.” The Examiner alleges it would have been obvious to modify Dravida to implement the input and output buffers of Figure 27 on separate line cards and states, “The motivation for doing so would have been to allow the nodes of Dravida to have more capacity (N input/output cards can support more traffic than if all the buffers were implemented on a single card)....” However, Applicant submits the Examiner does not present evidence to substantiate the assertion that “(N input/output cards can support more traffic than if all the buffers were implemented on a single card).”

Regarding claim 21, Applicant submits the cited portions of the cited reference fail to render obvious, as one example, “...wherein performing subsequent routing operations includes maintaining status of a plurality of transmit queues corresponding to a plurality of line cards in the switch, wherein the status is used to determine a non-congested compatible transmit queues for the subsequent routing operations.” The Examiner cites col. 5, lines 42-45, of Dravida et al. as allegedly indicating such feature. However, Applicant notes Dravida et al. state, in col. 11, lines 38-43, “The output of congestion monitor 2740 controls nodal processor 2730 such that a primary route to a destination is selected from table 2750 in absence of congestion and an alternate route to a destination is selected from table 2760 in the presence of congestion. Thus, Applicant submits the cited portion of the cited reference merely refers to selecting a primary route or an alternate route. Also, Applicant can find no reference to “performing subsequent routing operations” in the cited portion of the cited reference.

The Examiner has rejected claims 1, 2, 12, 13, 17, and 19-23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,838,677 to Kozaki et al. in view of U.S. Patent No. 5,802,040 to Park et al. Regarding claim 1, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, “...wherein the resource routing processor receives congestion indications and preferentially selects uncongested routes for subsequent connections within the communication switch based on the congestion indications.” The Examiner acknowledges, “Kozaki does not disclose the limitation of the resource routing processor.” The Examiner cites “(element 6 of Figure 1, see specifically element 13 of Figure 2)” of the Park reference as allegedly disclosing a “resource routing processor.” Regarding claim 2, Applicant submits the cited

portions of the cited references fail to teach or suggest, as one example, "...wherein the resource routing processor performs resource allocation amongst connections supported by the switch." The Examiner cites "(see lines 10-16 of column 4)" of the Park reference as allegedly disclosing the features of claims 1 and 2 noted above. However, Applicant submits the Park reference teaches away from such features, as well as features of claims 17, 19, 12, 13, and 20-23, for reasons consolidated following discussion of individual claims set forth below.

Regarding claim 17, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, "...a plurality of line cards operably couple to the routing control block, wherein each of the line cards includes at least one transmit queue, wherein when congestion is detected on a transmit queue, a congestion indication is provided to the routing control block such that calls are routed away from the congestion." Regarding claim 19, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, "...providing an indication of the congestion to a central control block that performs call processing and routing for a plurality of line cards included in the communication switch, wherein the central control block performs subsequent routing operations in a manner that avoids the congestion corresponding to the line card." The Examiner acknowledges Kozaki does not disclose the limitation of the routing control block or central control block. The Examiner cites "(element 6 of Figure 1, see specifically element 13 of Figure 2)" of the Park reference as allegedly disclosing a "routing control block" and a "central control block." The Examiner cites "(see lines 4-10 of column 14 and lines 7-9 of column 15)" of the Kozaki reference as allegedly disclosing other aspects of the features of claims 17 and 19 noted above.

Regarding claim 12, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, "...a plurality of line cards operably coupled to the multiprocessor control block, wherein the plurality of line cards include ingress and egress queuing points for line card data units, wherein when a congestion condition exists at a queuing point within a line card, a line card congestion indication is generated and provided to the resource routing processor such that the resource routing processor selects routes at least partially based on line card congestion indications received." The Examiner states, "...a line card congestion indication is generated (see lines 4-10 of column 14 and lines 7-9 of column 15 of Kozaki) and provided to the resource routing processor such that the resource routing processor selects routes at least partially based on line card congestion indications received (see lines 10-16 of column 4 of Park)."

Regarding claim 13, the Examiner states, "the combination of Kozaki and Park used in the rejection of parent claim 12 also discloses the limitation of a message processor...." Applicant has presented arguments as to why it would not have been obvious to combine the cited portions of the cited references to allegedly yield the features of claim 12, as Applicant submits the cited portions teach away from such combination for reasons consolidated following individual claim arguments set forth below. Likewise, Applicant submits the cited portions teach away from a combination that would allegedly render obvious claim 13. Moreover, Applicant

submits the Examiner does not appear to have alleged, with respect to claim 12, any teaching or suggestion of certain features of claim 13, for example, a “plurality of intermediate processors.”

Regarding claim 20, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, “...wherein the central control block includes a resource routing processor, a plurality of intermediate processors, and a link layer processor, wherein the resource routing processor performs the subsequent routing operations.” The Examiner cites “(element 13 of Figure 2 of Park)” as allegedly teaching or suggesting “a resource routing processor,” “(elements 12, 21-23, and 31-33 of Figure 2 of Park)” as allegedly teaching or suggesting “a plurality of intermediate processors,” and “(element 20 and 30 of Figure 2 of Park)” as allegedly teaching or suggesting “a link layer processor.” Applicant can find no mention in the cited portion of the cited reference of either element 20 or 30 being a “link layer processor.” Moreover, Applicant notes element 20 is depicted as comprising elements 21-13, and element 30 is depicted as comprising elements 31-33. Thus, Applicant submits the Examiner has failed to show Figure 2 of the Park reference as teaching “...wherein the central control block includes...a plurality of intermediate processors, and a link layer processor....” Furthermore, Applicant notes the Examiner cites, with respect to base claim 19, “(element 6 of Figure 1, see specifically element 13 of Figure 2)” of the Park reference as allegedly disclosing a “central control block.” Thus, Applicant submits the Examiner has failed to show the cited portions of the Park reference as allegedly disclosing “...wherein the central control block includes a resource routing processor, a plurality of intermediate processors, and a link layer processor....”

Regarding claim 21, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, “...wherein performing subsequent routing operations includes maintaining status of a plurality of transmit queues corresponding to a plurality of line cards in the switch, wherein the status is used to determine a non-congested compatible transmit queues for the subsequent routing operations.” The Examiner cites “(lines 10-16 of column 4)” as allegedly disclosing the features of claim 21. The Examiner states, “The routing table represents the...status and the link being affordable suggests that it doesn’t contain a congestion status.” Applicant submits the Examiner provides no evidence to support the assertion that “The routing table represents the...status....” On the contrary, Applicant notes col. 4, lines 11-13, state, “...the routing controller 13 retrieves a routing table which is set when a system is started....” Also, the Examiner provides no evidence to support the assertion that “...the link being affordable suggests that it doesn’t contain a congestion status.”

Regarding claim 22, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, “...prioritizing data flow in the switch such that congestion is concentrated at the plurality of transmit queues.” The Examiner cites lines 26-33 of column 10 of the Kozaki reference as allegedly disclosing the features of claim 22. However, Applicant submits the cited portion of the Kozaki reference teaches away from the features of claim 22. Applicant notes col. 10, lines 26-33, of the Kozaki reference merely states, “In the method of this embodiment, if there is no queue in the congestion state in the switch, the cell is read from the

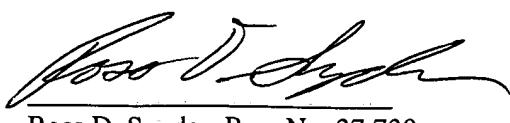
input buffer 25 in the queue designated by the bandwidth control table 264 (if a plurality of queues are designated, the queue having the highest priority is selected). If there is a queue in the congestion state, a cell is read from the output buffer [sic], which cell is not in the congestion queue among the queues designated by the bandwidth control table 264." Applicant notes the phrase "highest priority" appears in reference to "If there is no queue in the congestion state..." and does not appear to disclose "...prioritizing data flow in the switch such that congestion is concentrated at the plurality of transmit queues."

Regarding claim 23, Applicant submits the cited portions of the cited references fail to teach or suggest, as one example, "...wherein the congestion in the transmit queue is a result of a buildup of messages corresponding to programming commands that are directed towards the line card." The Examiner cites buffer 38 of Figure 9 of the Kozaki reference as allegedly disclosing the features of claim 23. However, Applicant submits buffer 38 of Figure 9 of the Kozaki reference merely bears the label "BUFFER." Accordingly, Applicant can find no teaching in the cited portion of the cited reference as to buffer 38 of Figure 9 of the Kozaki reference allegedly teaching "...wherein the congestion in the transmit queue is a result of a buildup of messages corresponding to programming commands that are directed towards the line card."

Regarding claims 1, 2, 12, 17, 19, and 20-23, for example, Applicant notes Fig. 2 of the Park reference identifies routing controller 13 receiving a "ROUTING REQUEST" from congestion controller 12 and col. 4, lines 10 and 11, of the Park reference state, "If the routing request signal is received from the congestion controller 12,..." Regarding claims 2, 12, 17, 19, and 20-23, Applicant also notes lines 7-9 of column 15 of the Kozaki reference state, "...the congestion information may be transferred to the control point only when a congestion is detected." As the cited portion of the Kozaki reference refers to transfer of "congestion information," and the cited portion of the Park reference refers to receiving a "routing request signal," Applicant submits the cited portions of the cited references cannot be combined to allegedly teach or suggest the features of claims 2, 12, 17, 19, and 20-23. Furthermore, Applicant submits the Examiner does not appear, with respect to claims 1, 2, 12, 13, 17, and 20-23, to assert motivation to allegedly modify the purported teachings of the cited references so as to allegedly render the features of claim 1 obvious. Thus, Applicant submits the Examiner has not presented a *prima facie* showing of obviousness in accordance with MPEP § 2143.

Respectfully submitted,

11/22/2006  
Date



Ross D. Snyder, Reg. No. 37,730  
Attorney for Applicant(s)  
Ross D. Snyder & Associates, Inc.  
PO Box 164075  
Austin, Texas 78716-4075  
(512) 347-9223 (phone)  
(512) 347-9224 (fax)